

Fig 1

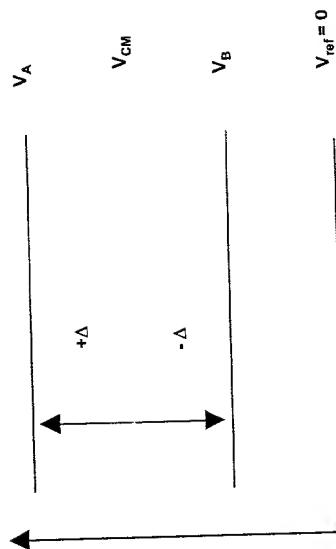


Fig 2

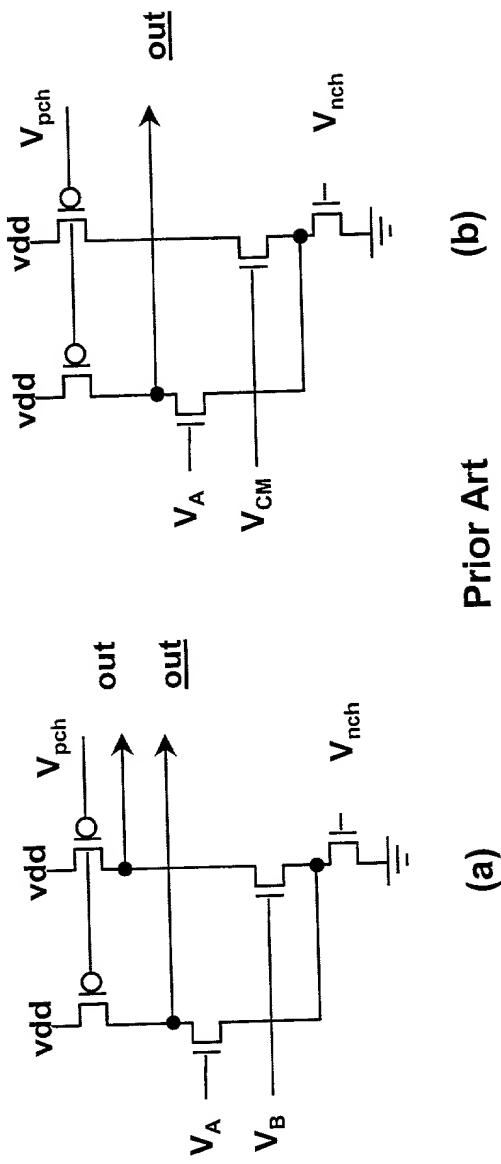


Fig 3

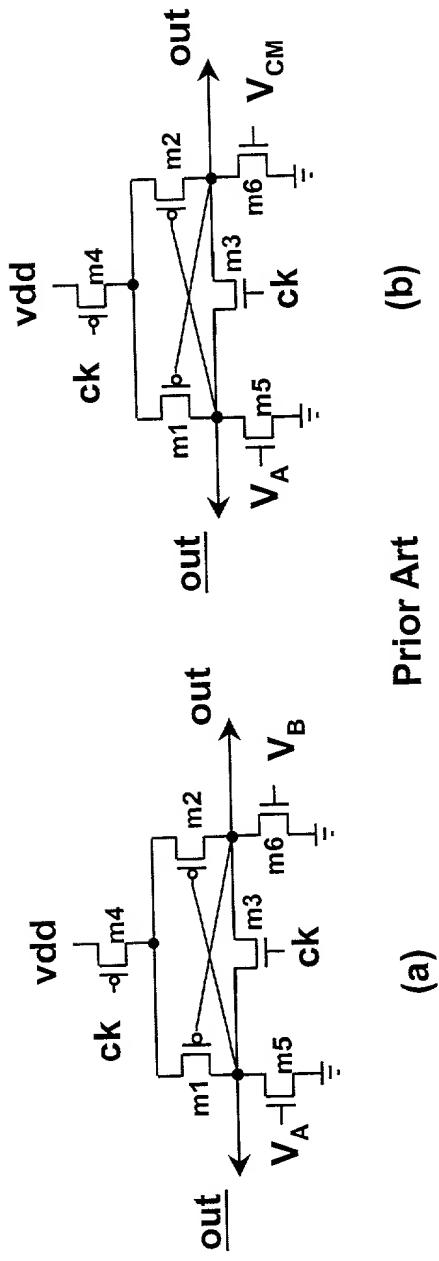


Fig 4

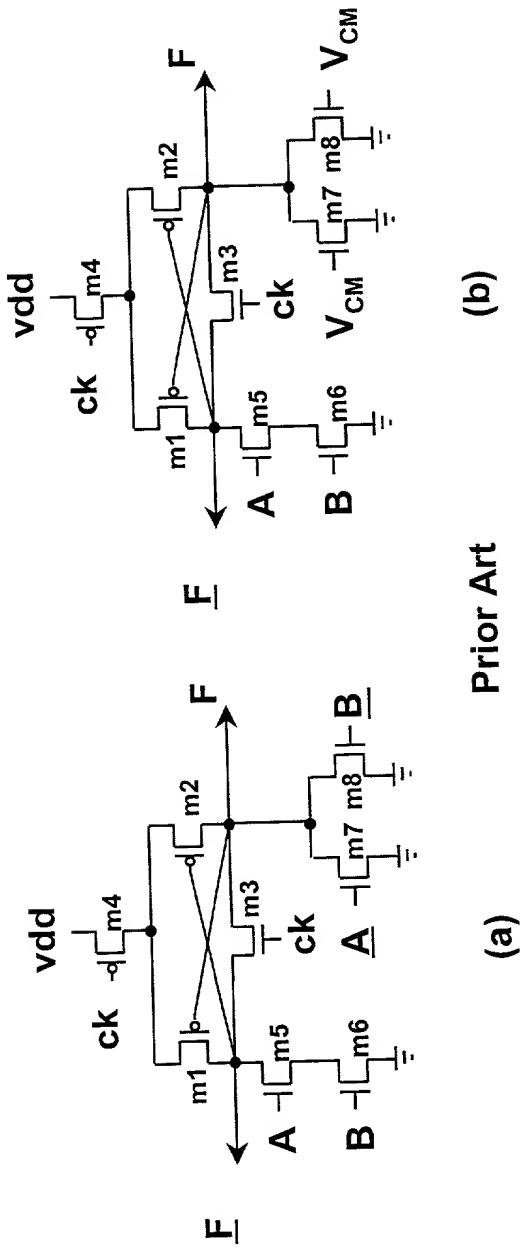
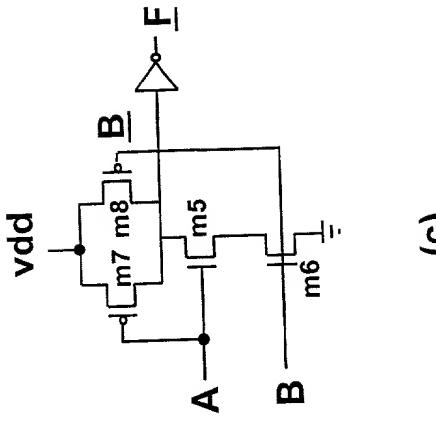
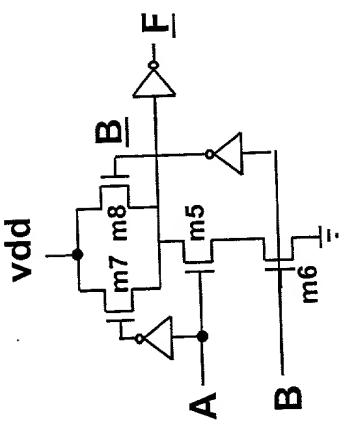
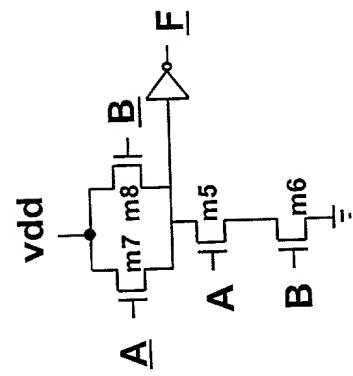
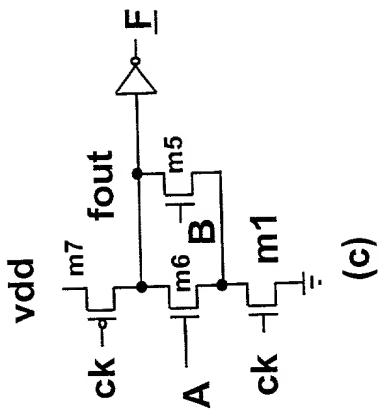
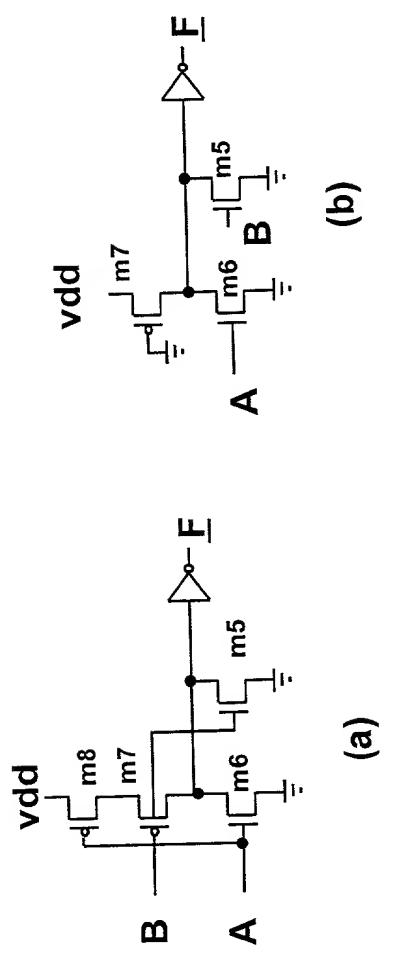


Fig 5



Prior Art

Fig 6



Prior Art

Fig 7

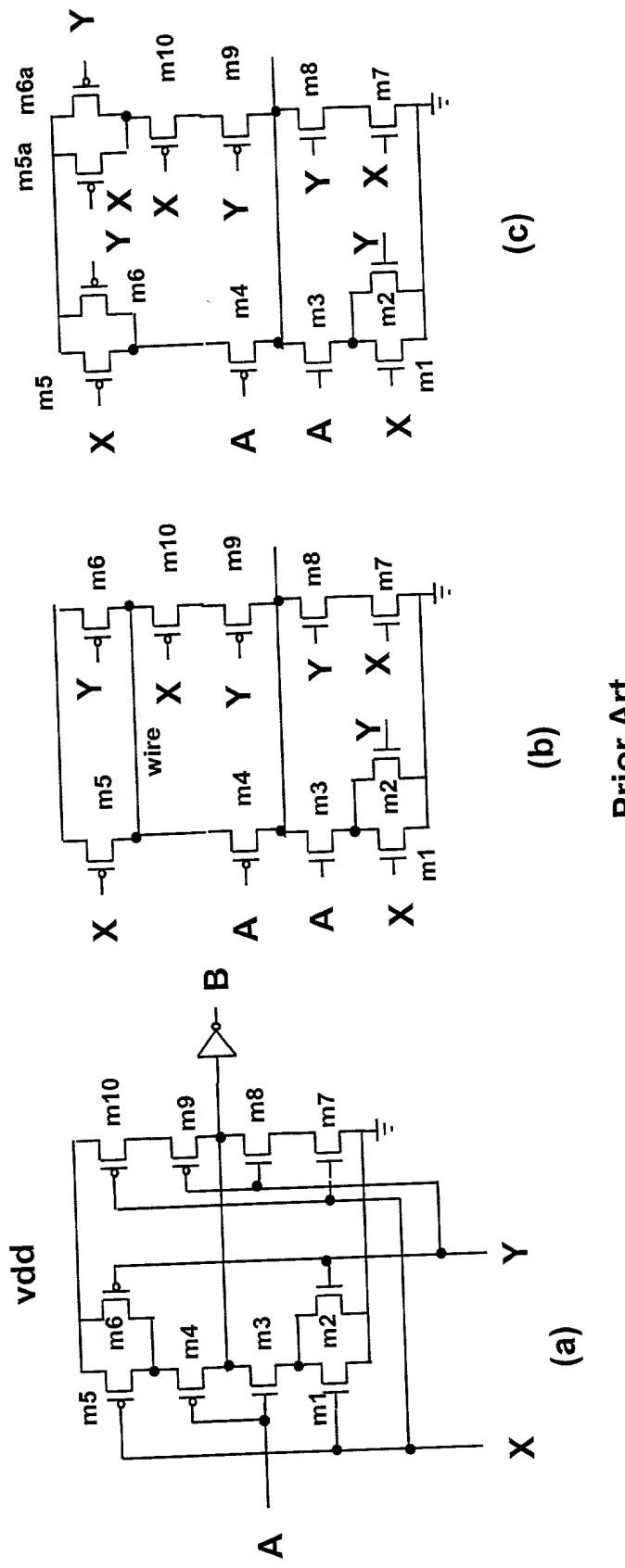


Fig 8

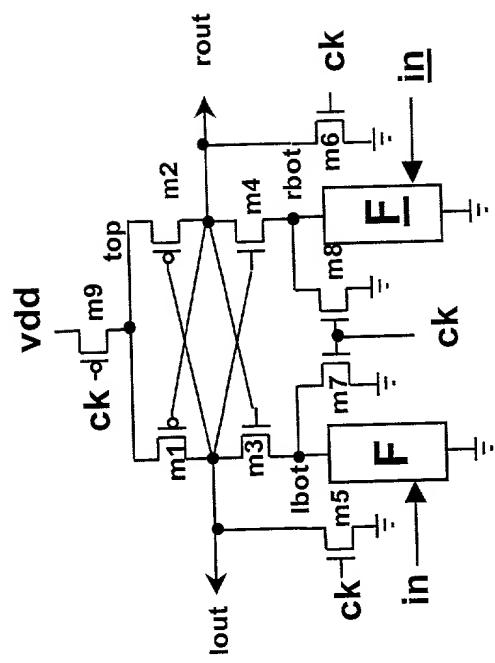


Fig 9

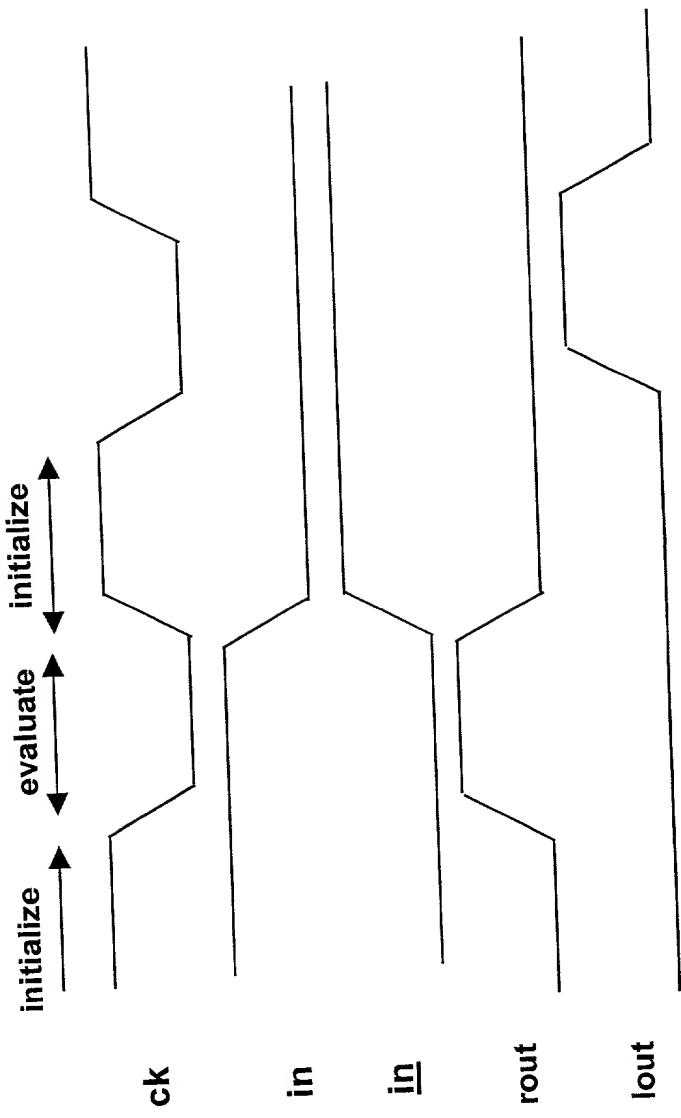


Fig 10A

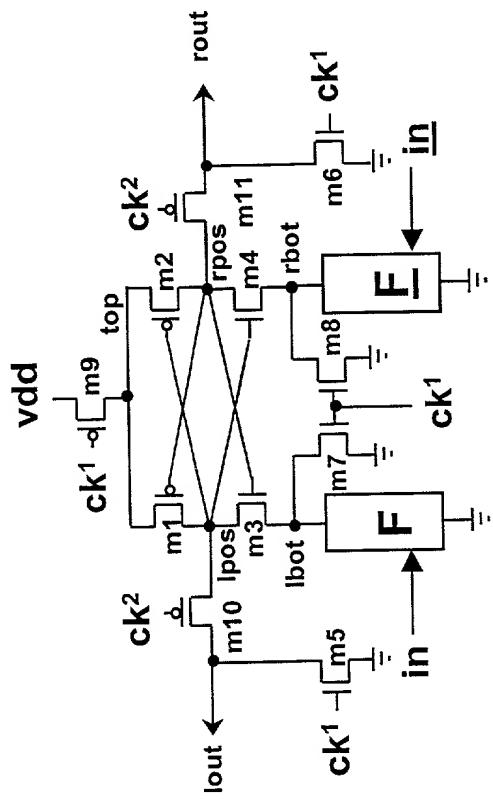


Fig 10B

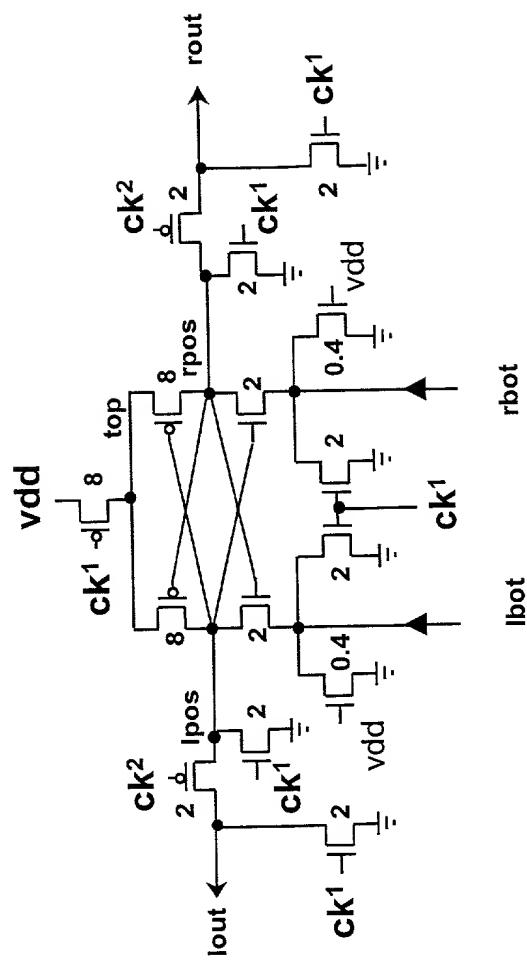


Fig 10C

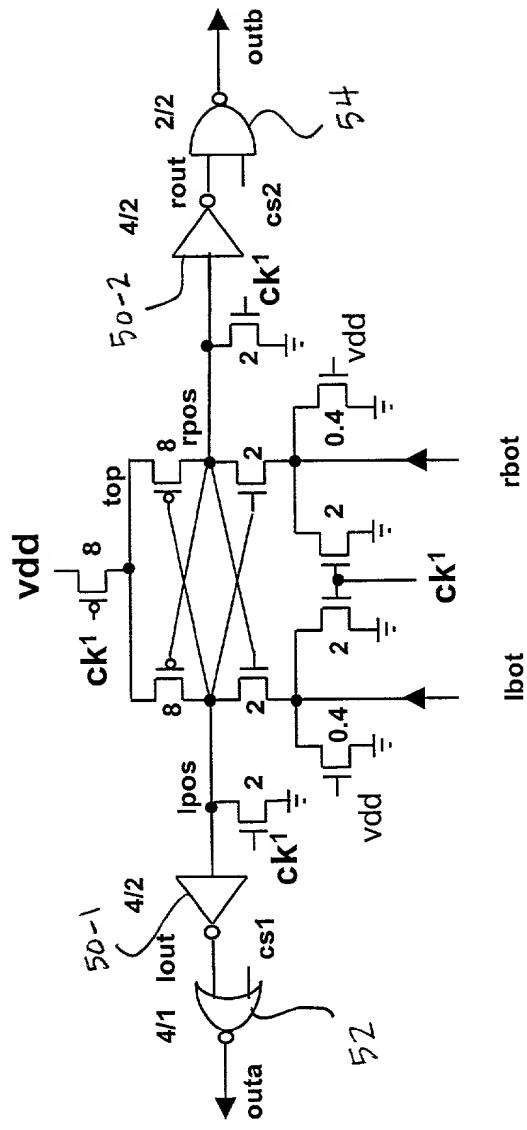


Fig 10D

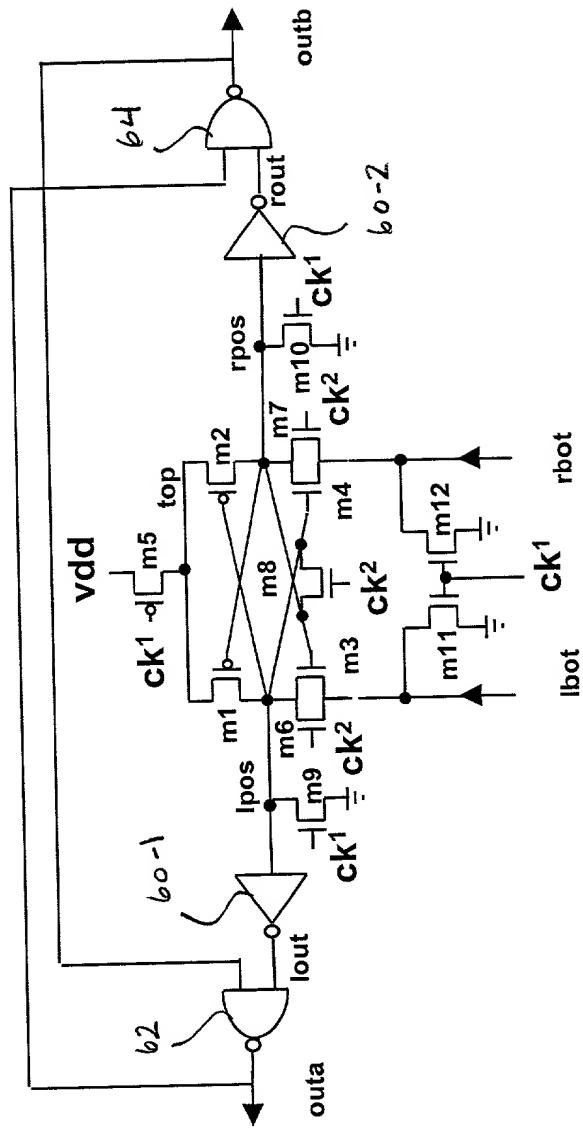


Fig 11

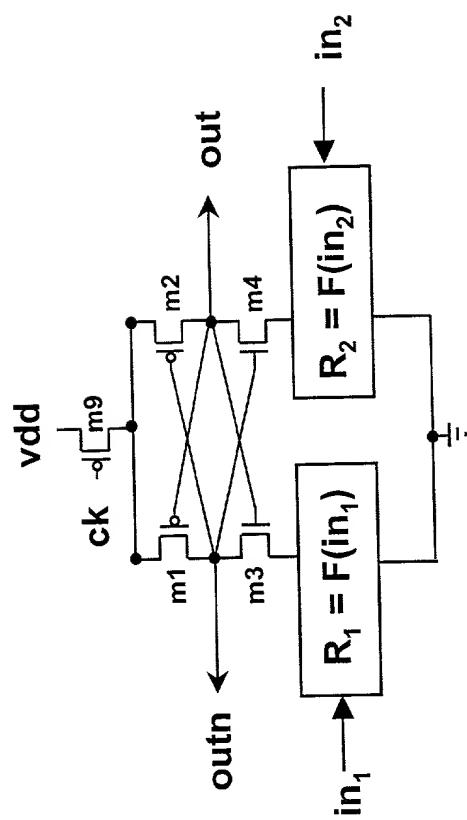


Fig 12

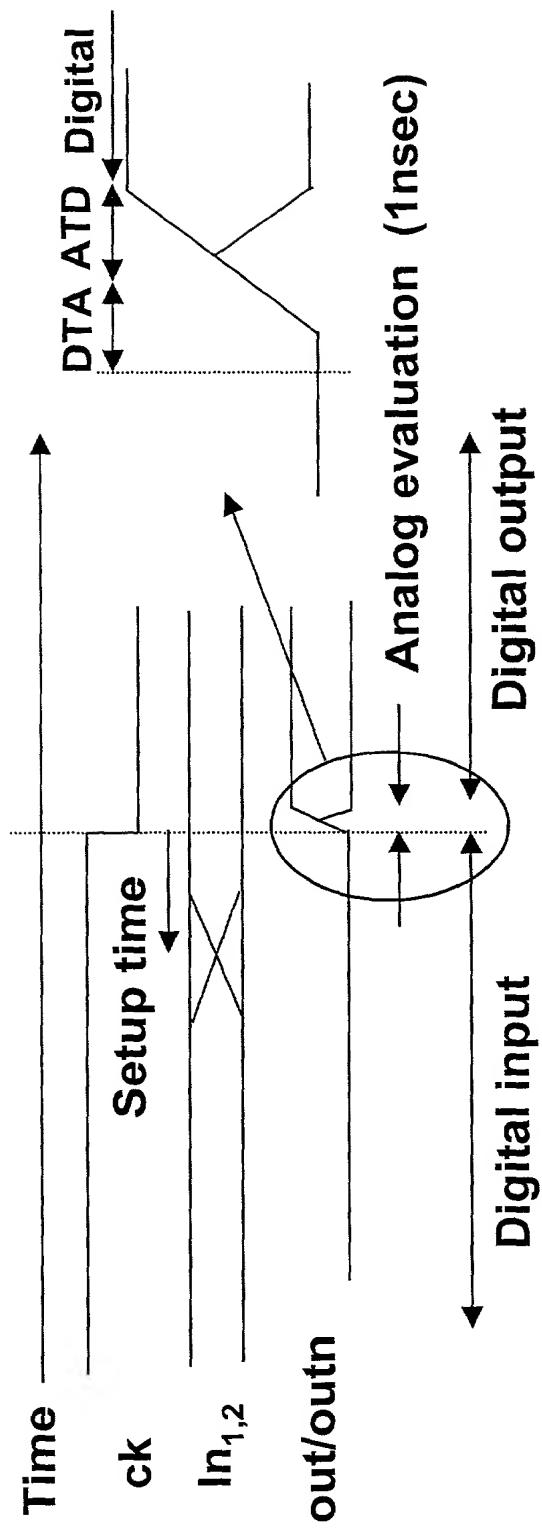


Fig 13

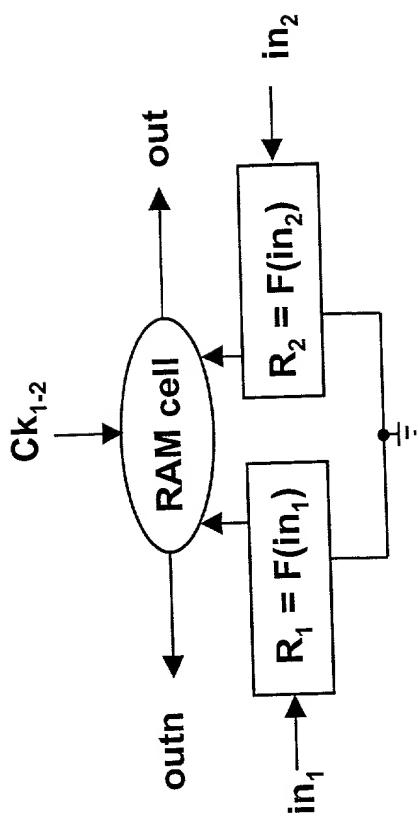


Fig 14

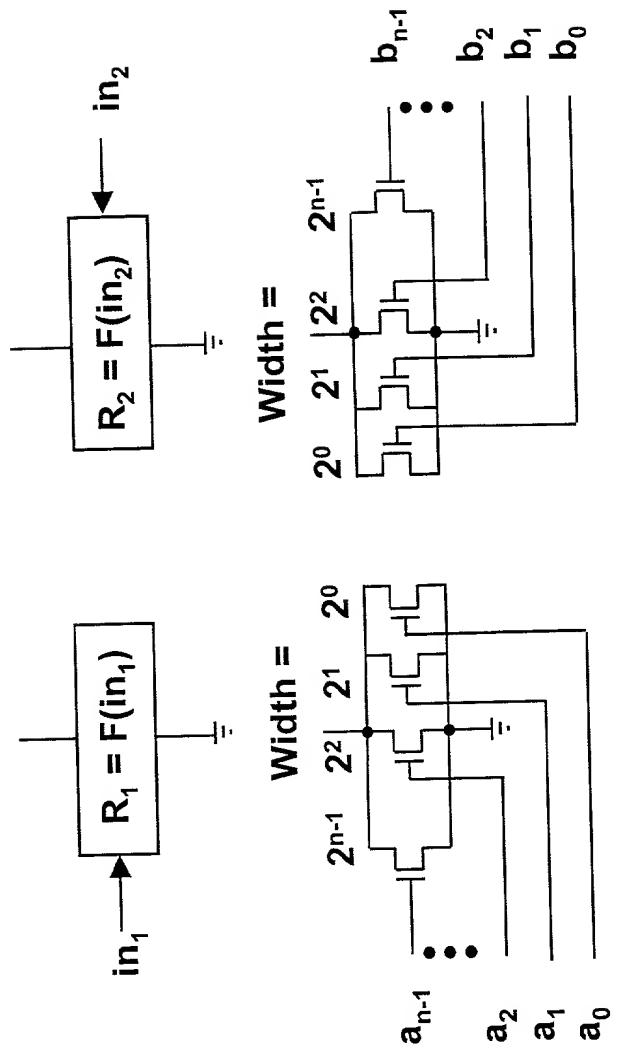


Fig 15

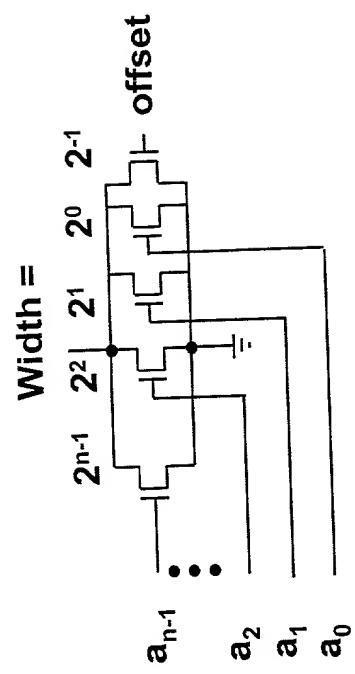


Fig 16

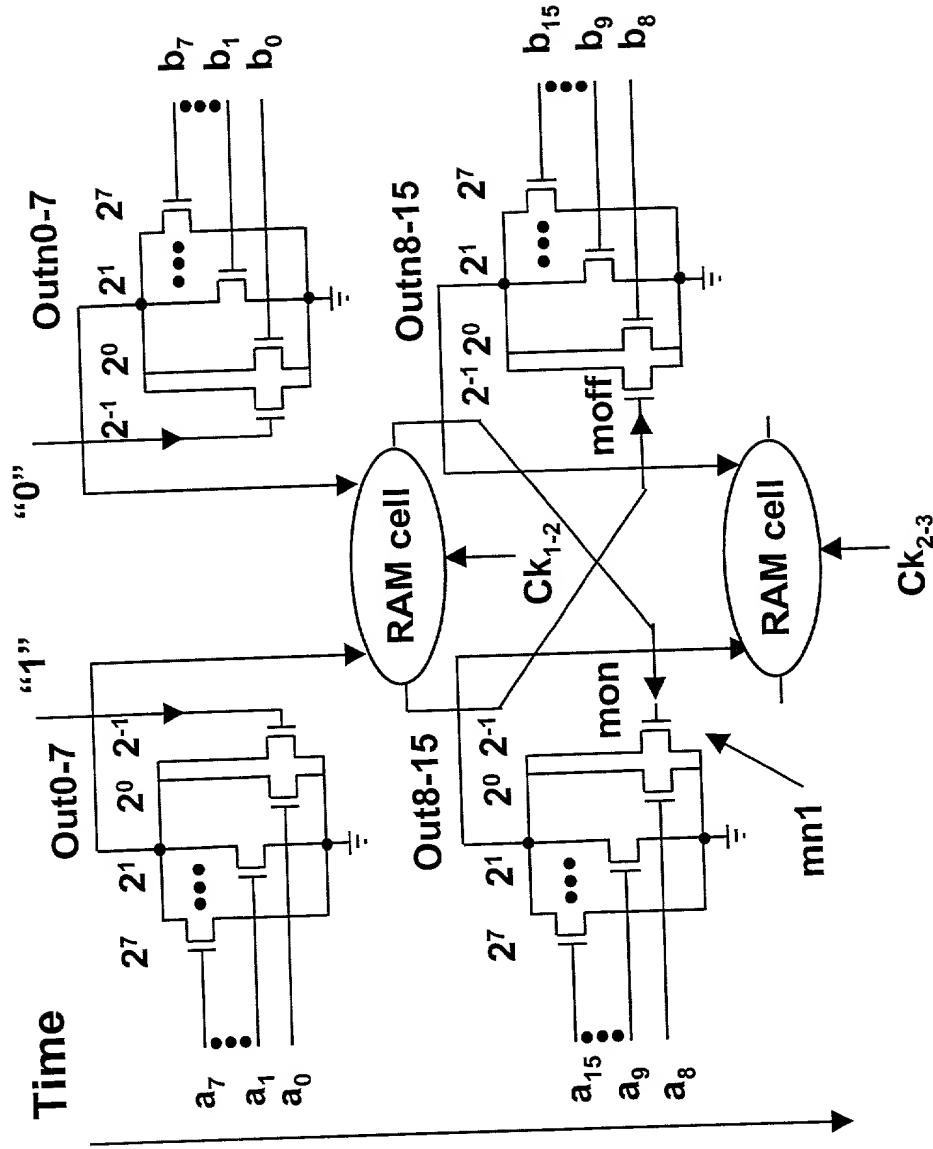


Fig 17

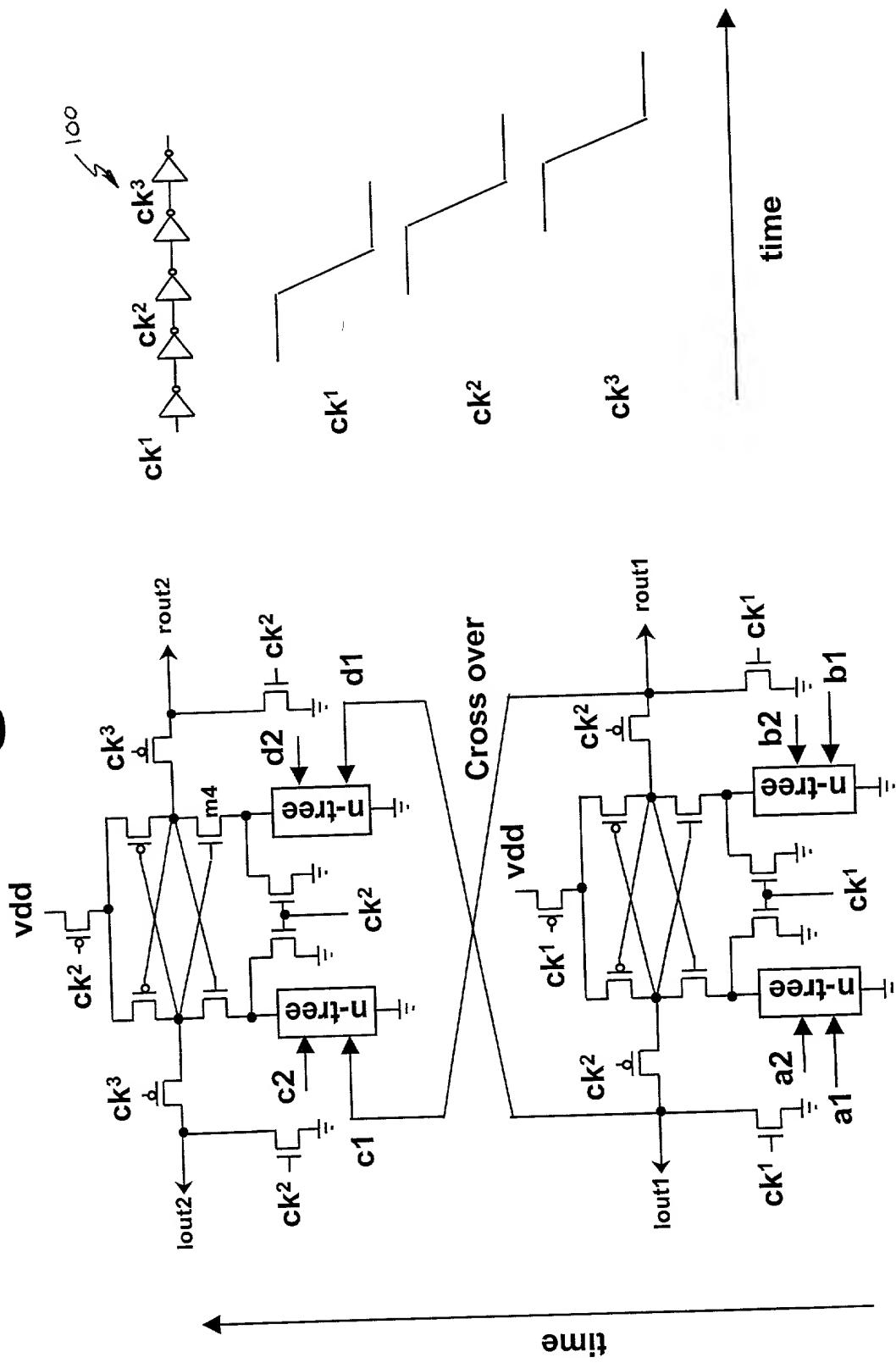


Fig 18

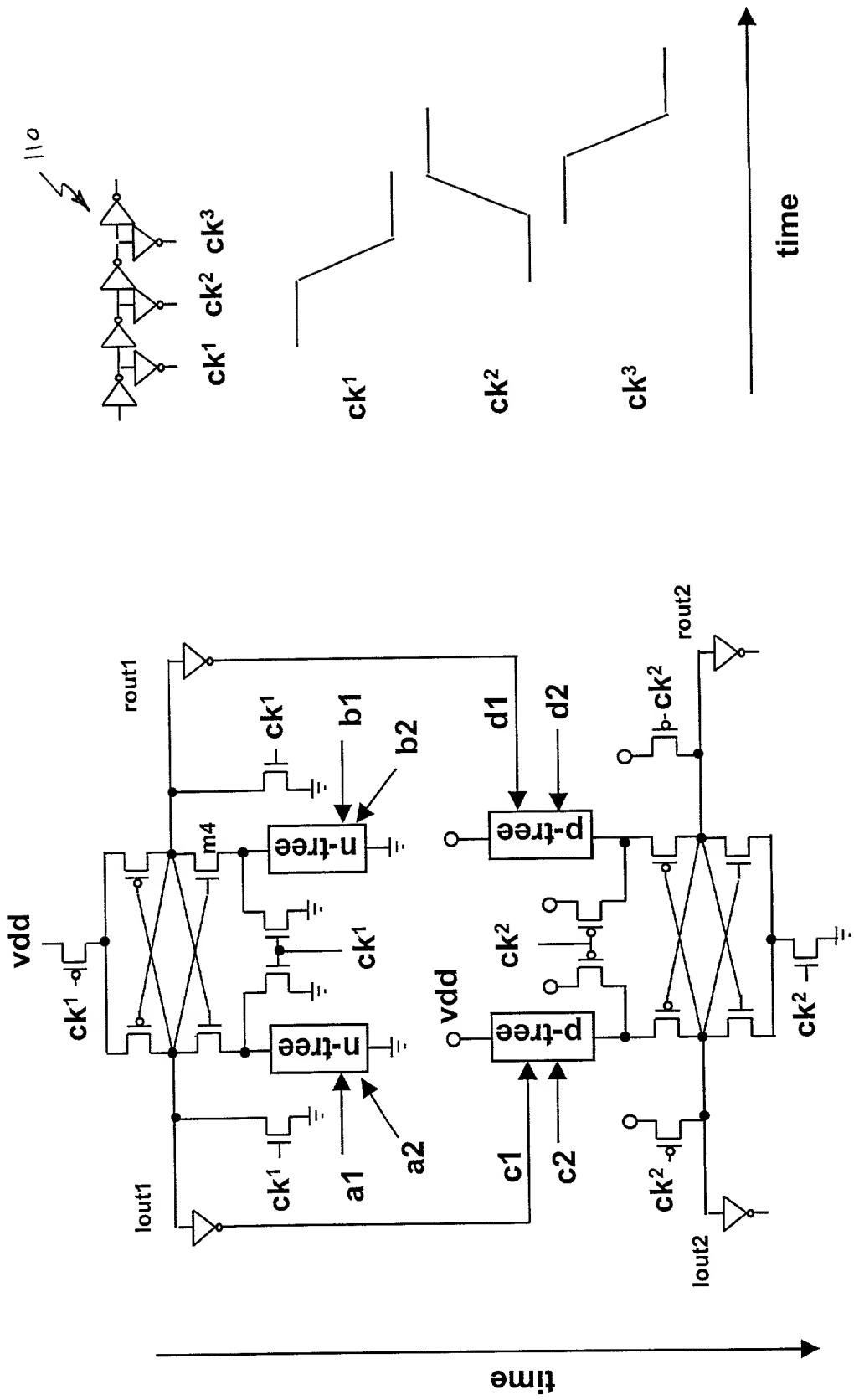


Fig 19

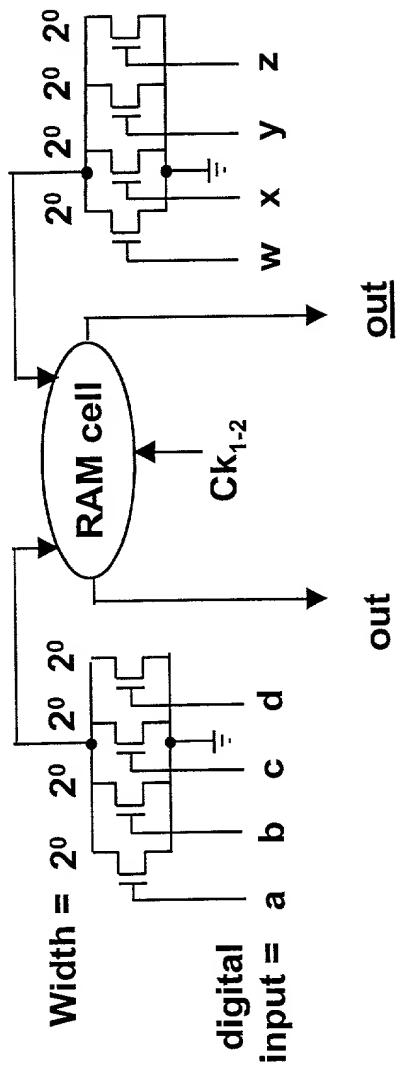


Fig 20

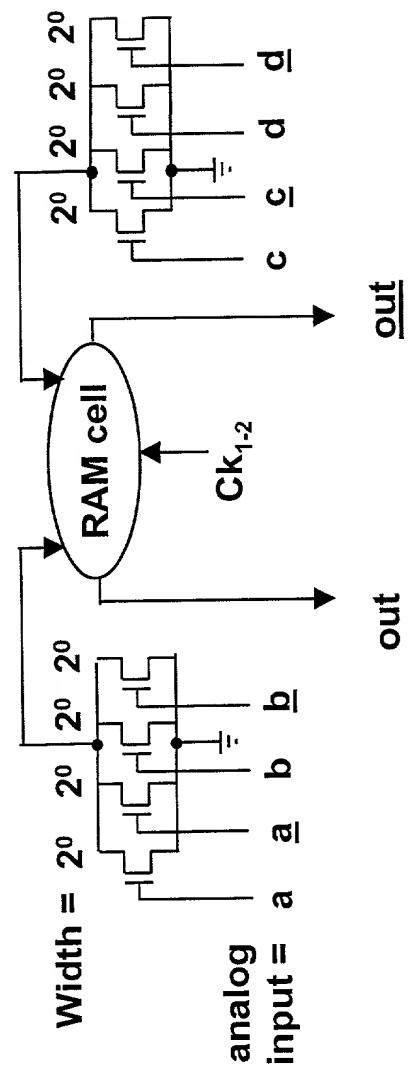


Fig 21

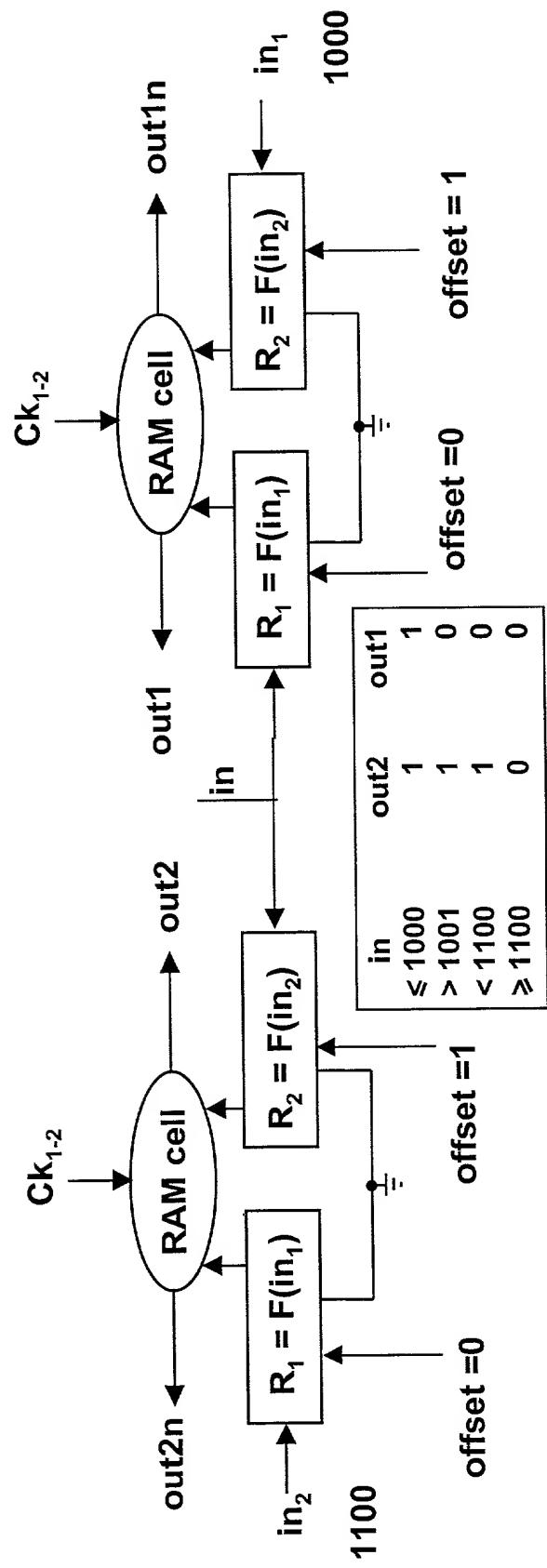


Fig 22

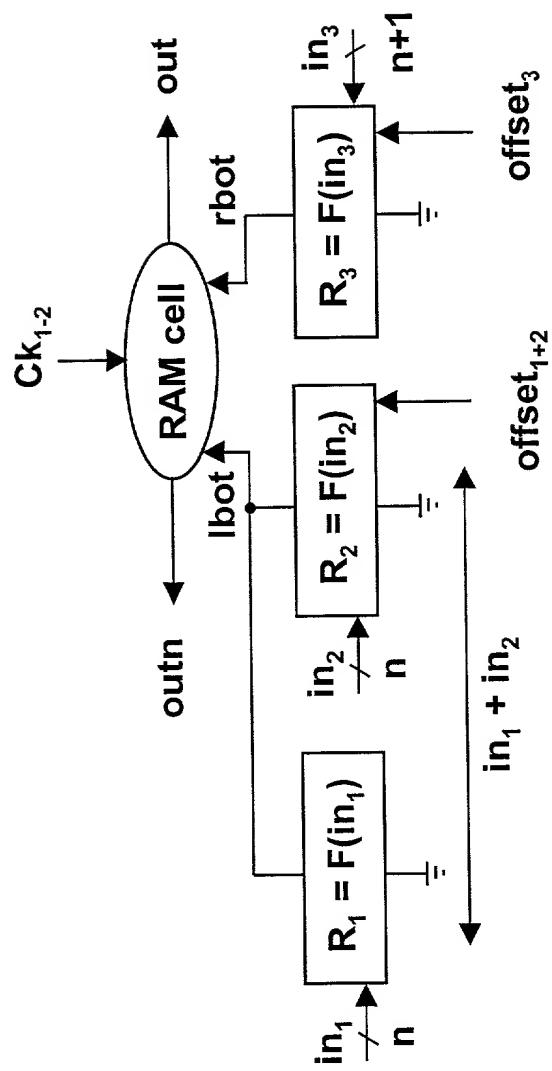


Fig 23

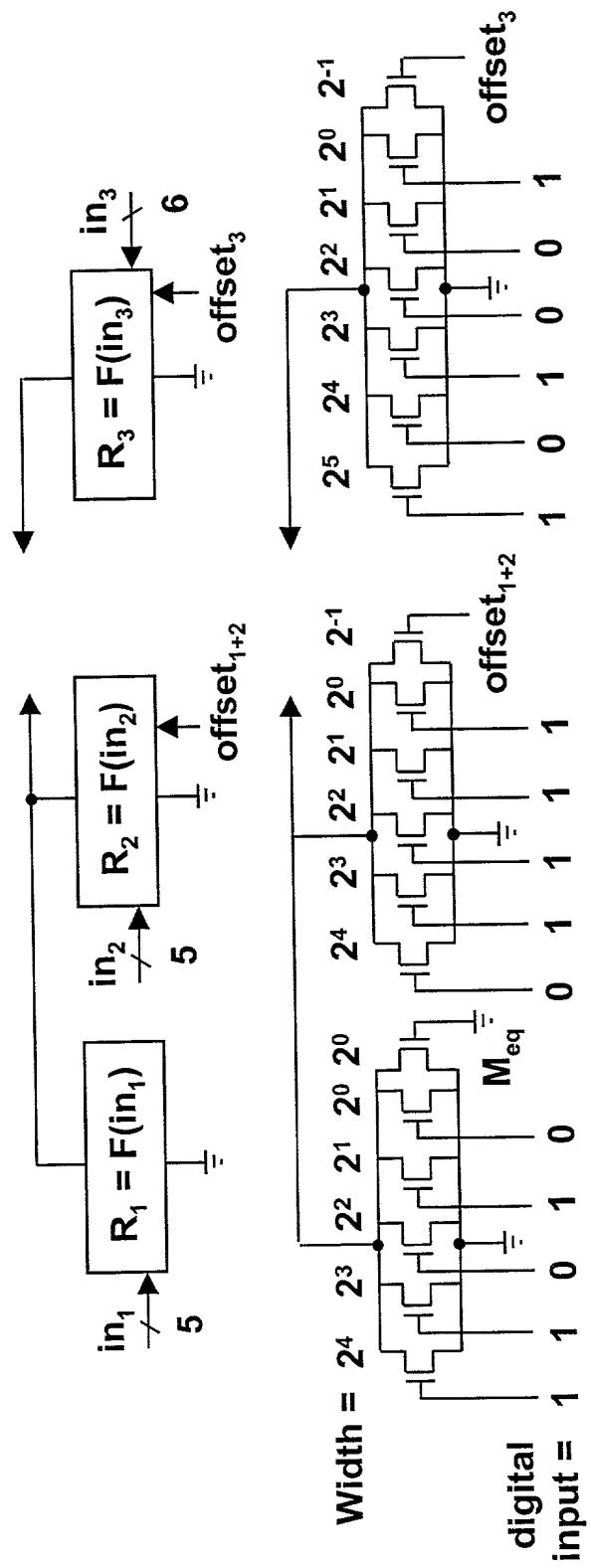


Fig 24A

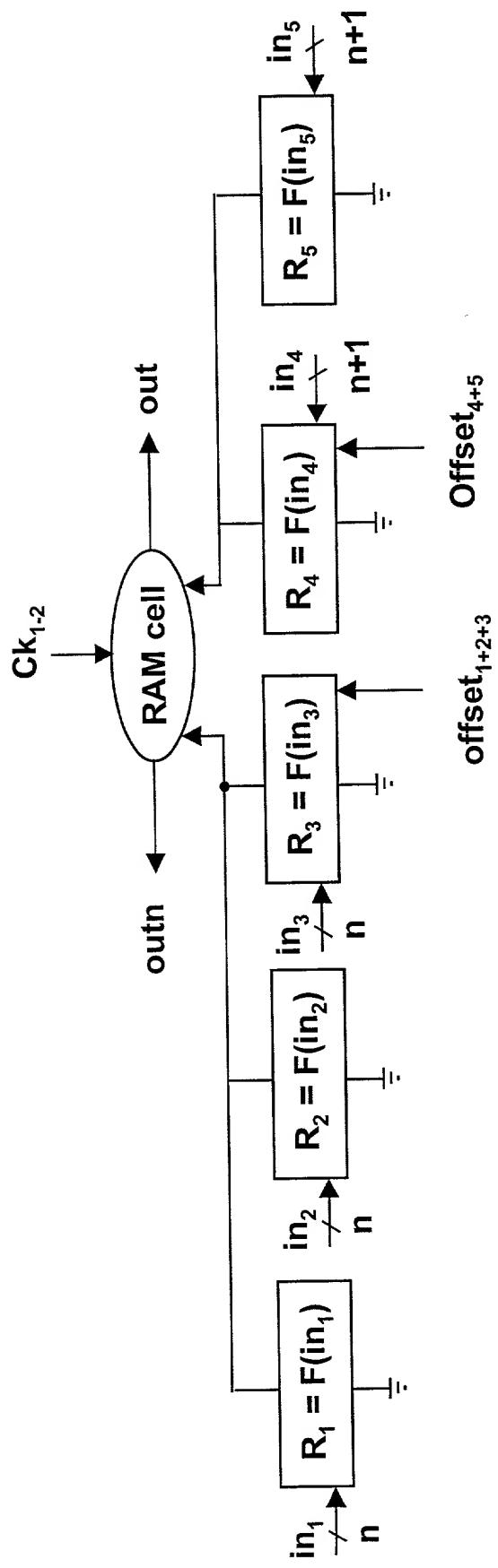


Fig 24B

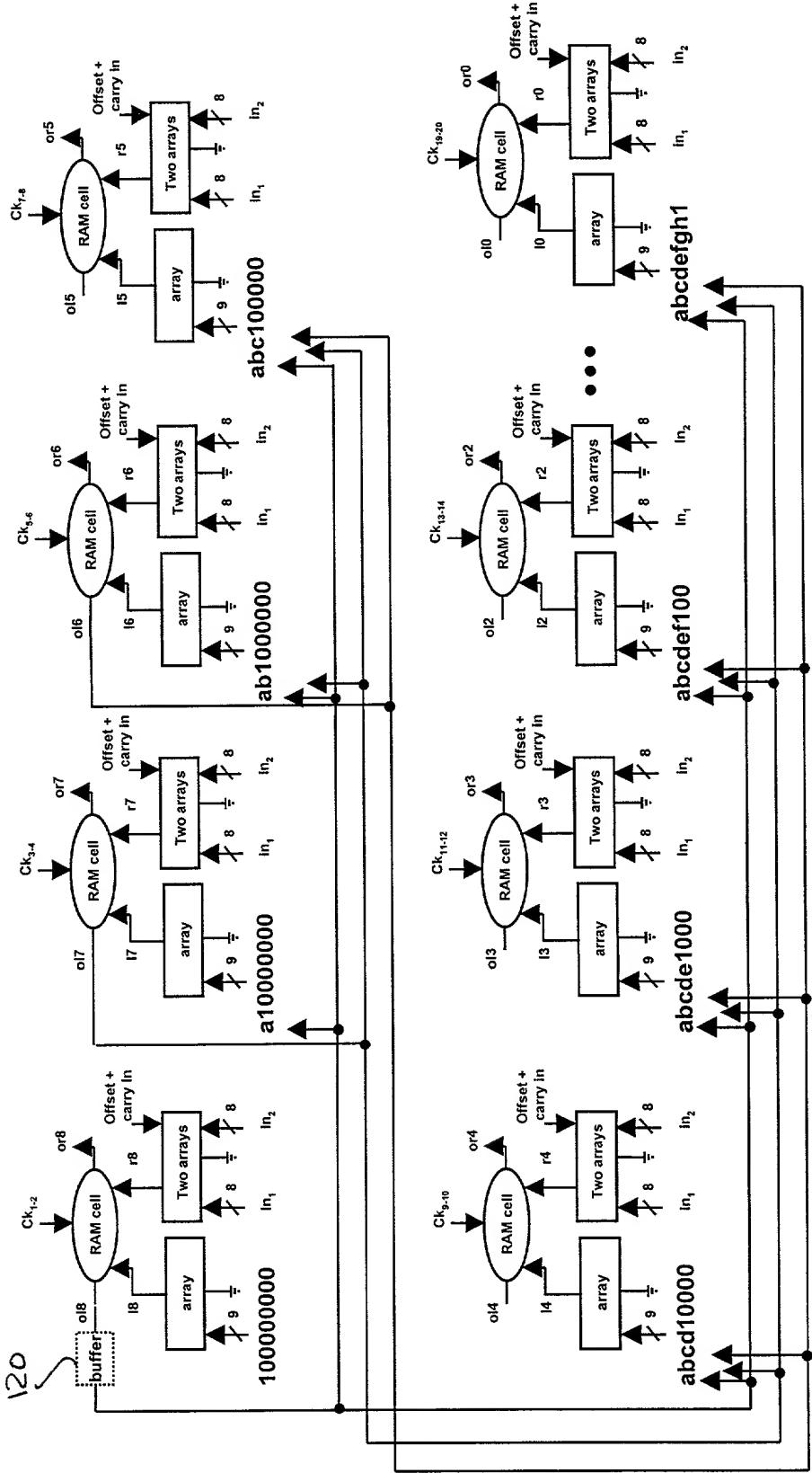


Fig 25

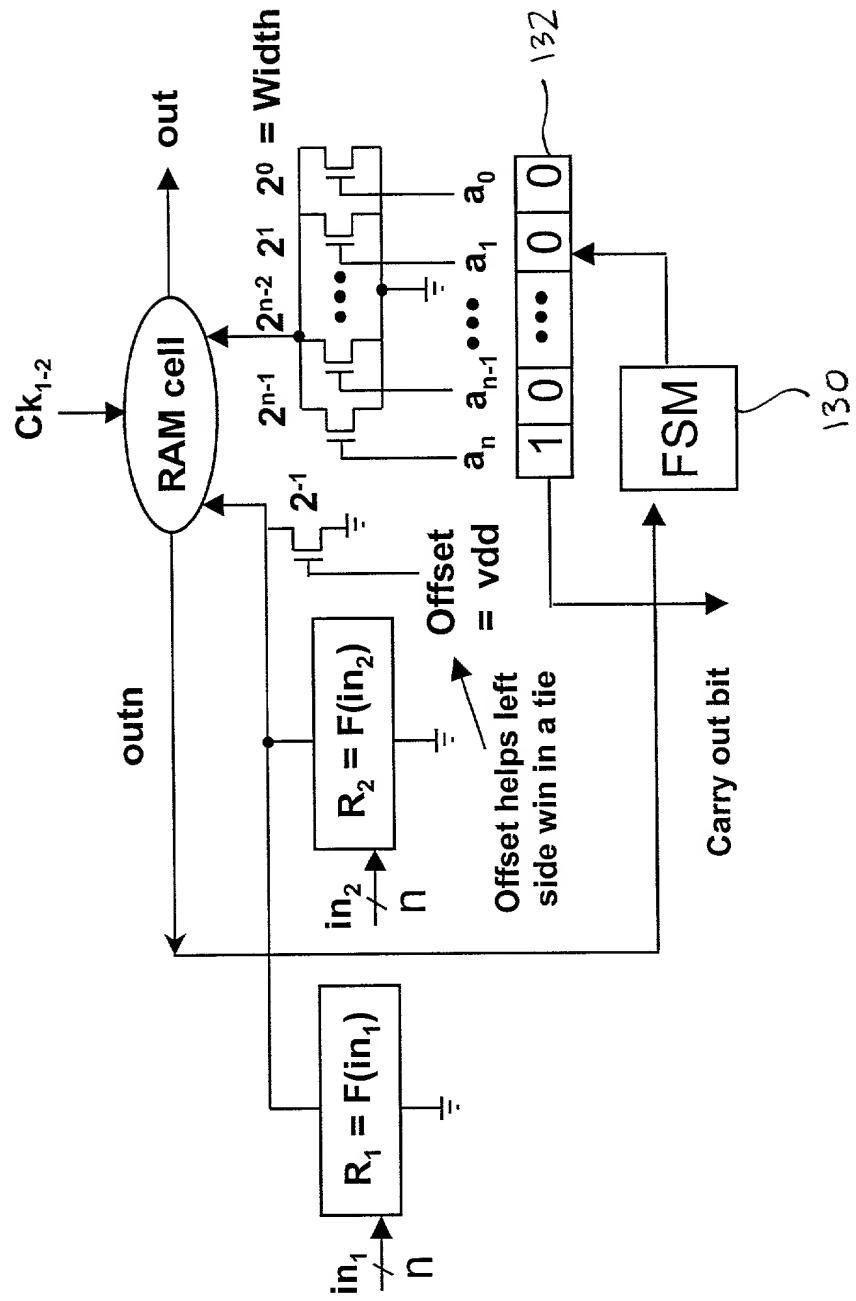


Fig 26

```
/* initialize */
n=8 ;
a[n] = 1;
for (k=1; k< n; k++)
a[k]=0;

for (i=0; i<n; ++i) /* i = clock tick */
if (out = 0)
a[n-i-1]=1;
else {
a[n-i] = 0;
if (i < n - 1)
a[n-i-1] = 1;
}
/* addition result is in array a[n] */
```

Fig 27

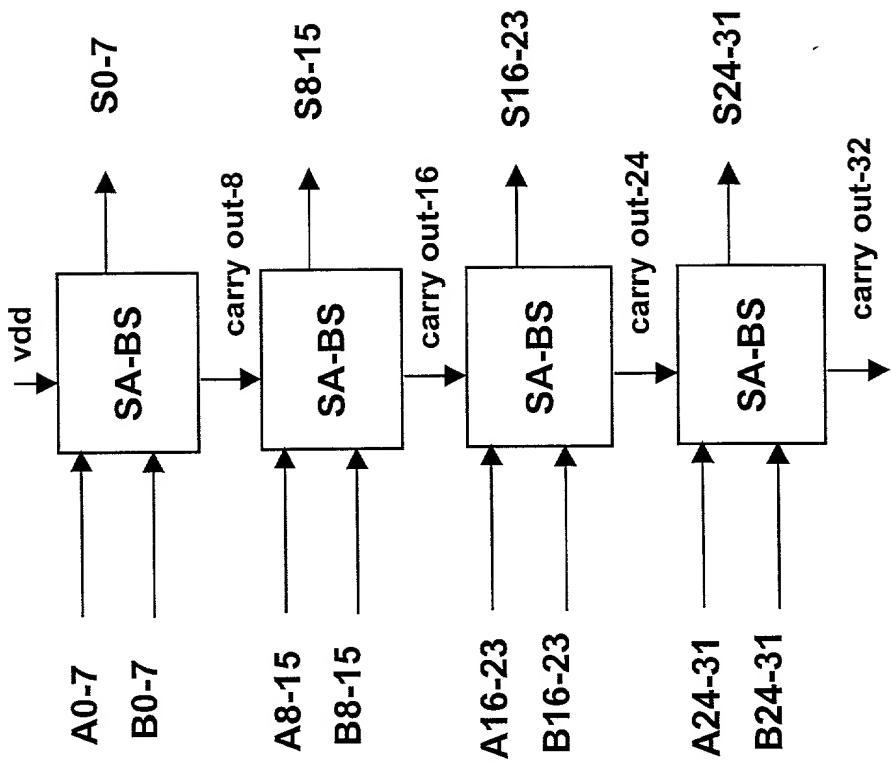


Fig 28

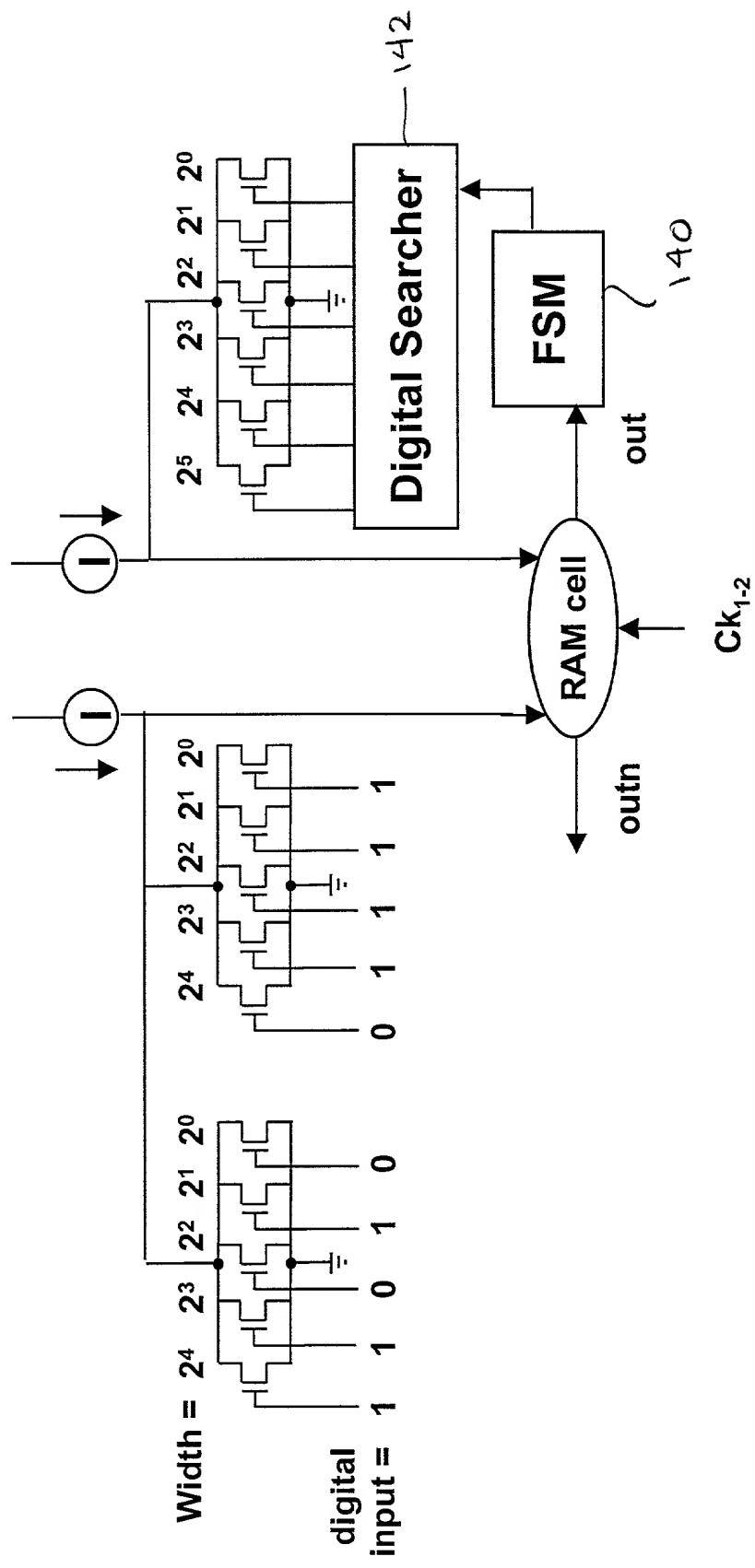
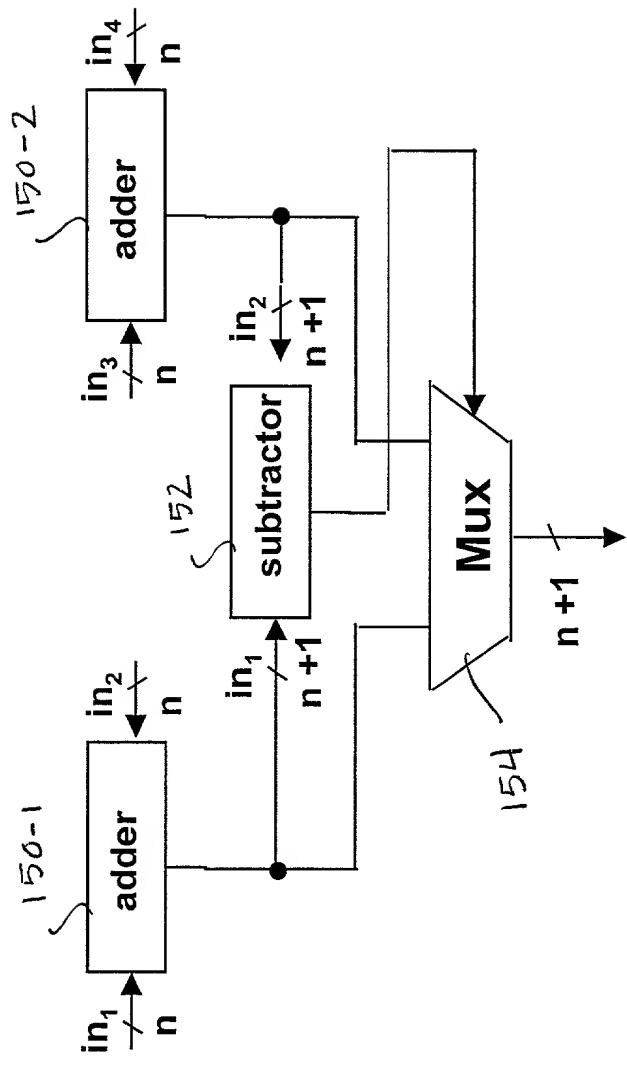


Fig 29



Prior Art

Fig 30

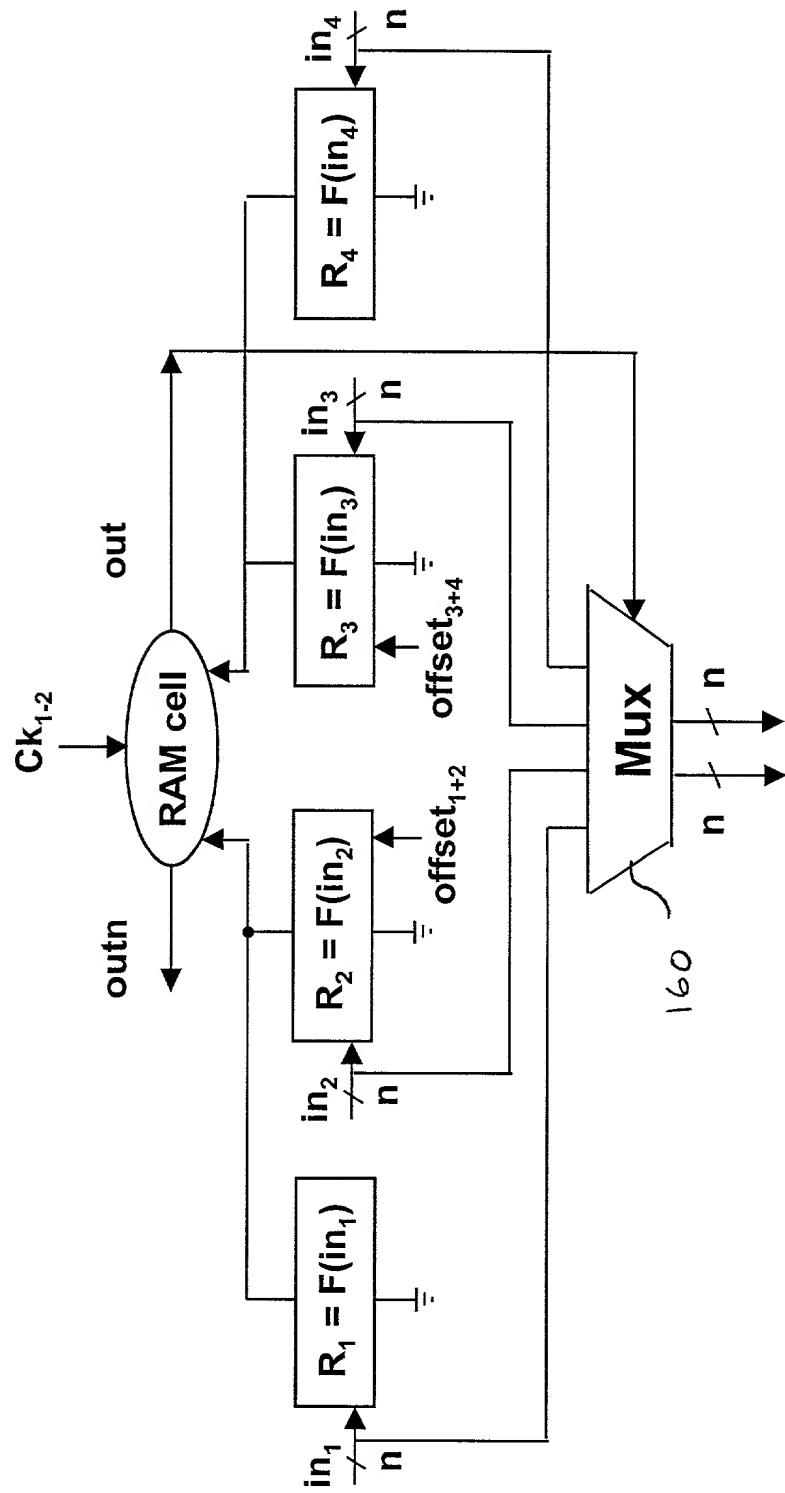


Fig 31

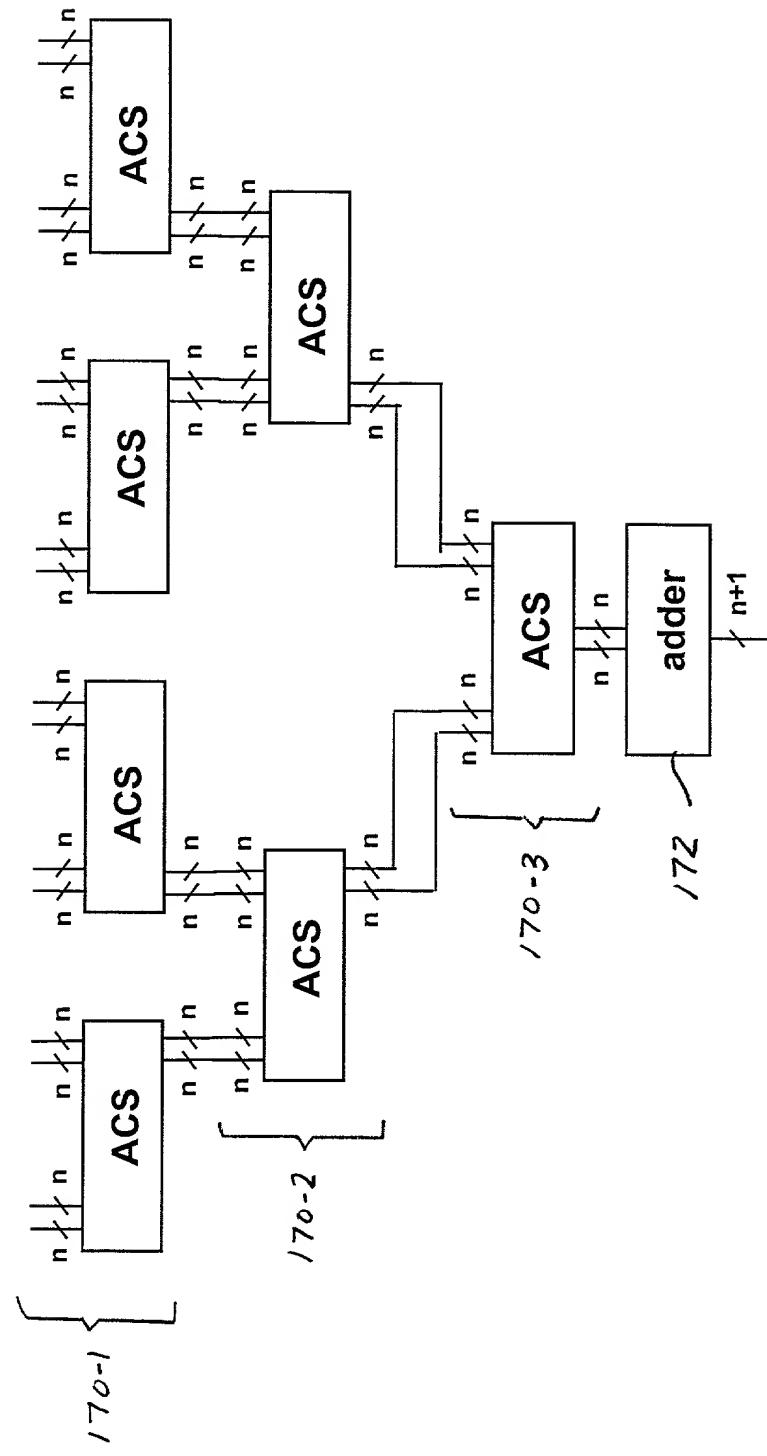


Fig 32

	POWER (μ W)	TRANSISTOR COUNT	DELAY (pSEC)
	Add	Select	Add
	Compare	Compare	Compare
Conventional	2000	200	5215
SeeSaw	100	300	55
Gain Factor	X20	X0.66	X95
			X0.54
			X2.17
			X1.15
			173
			200

Fig 33

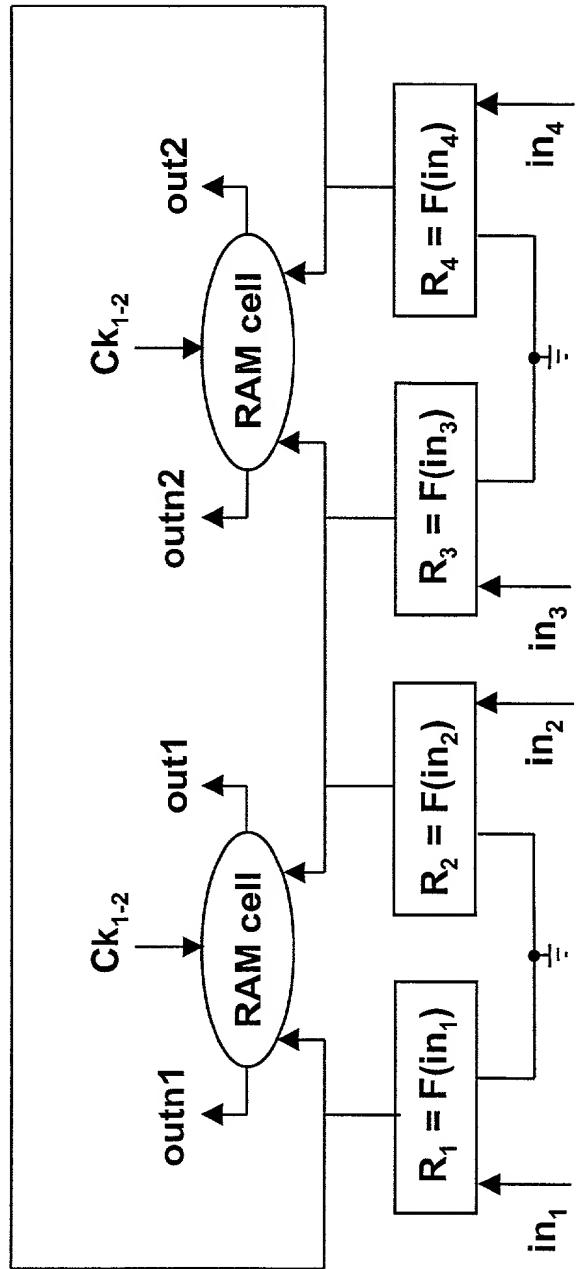


Fig 34

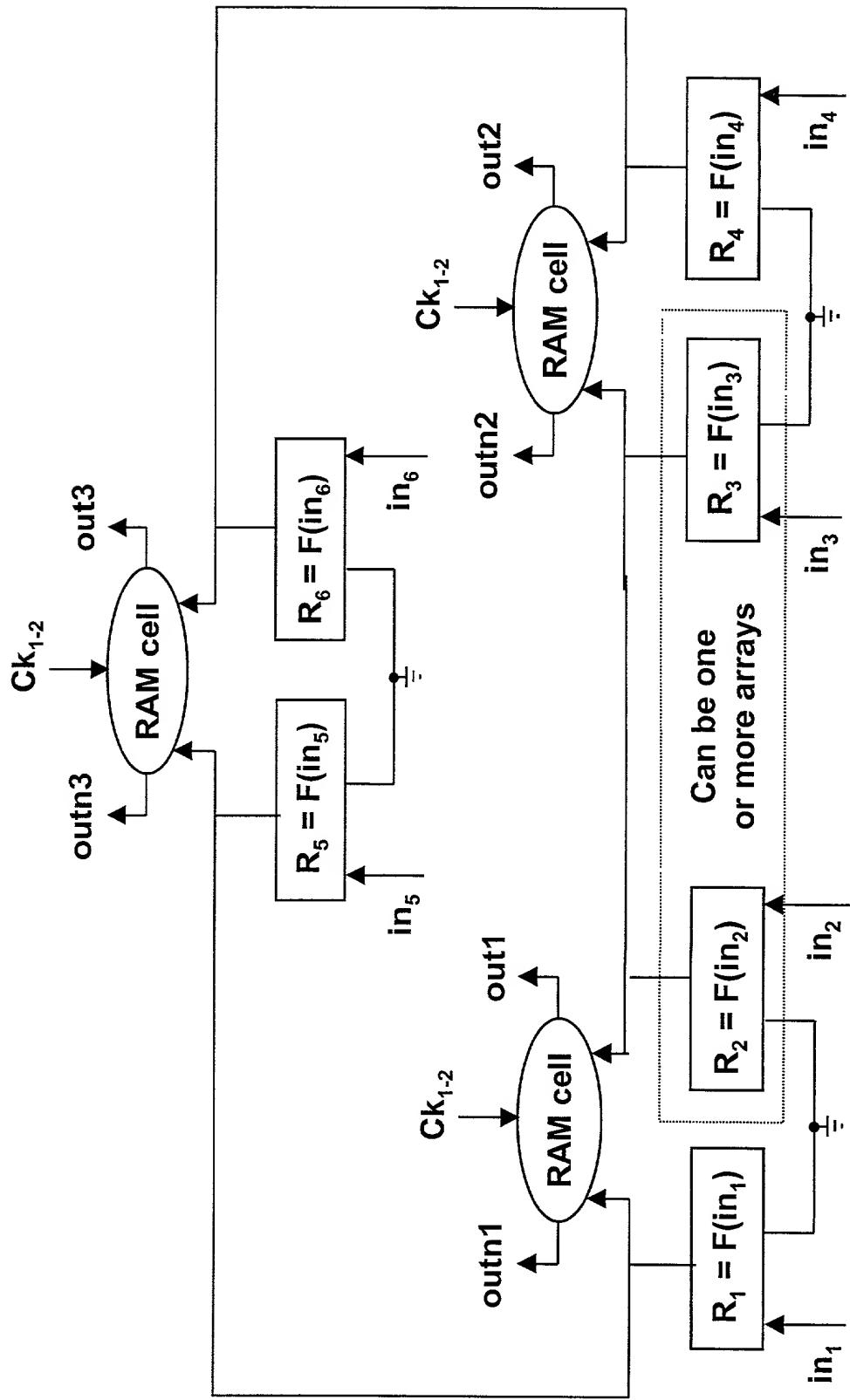


Fig 35

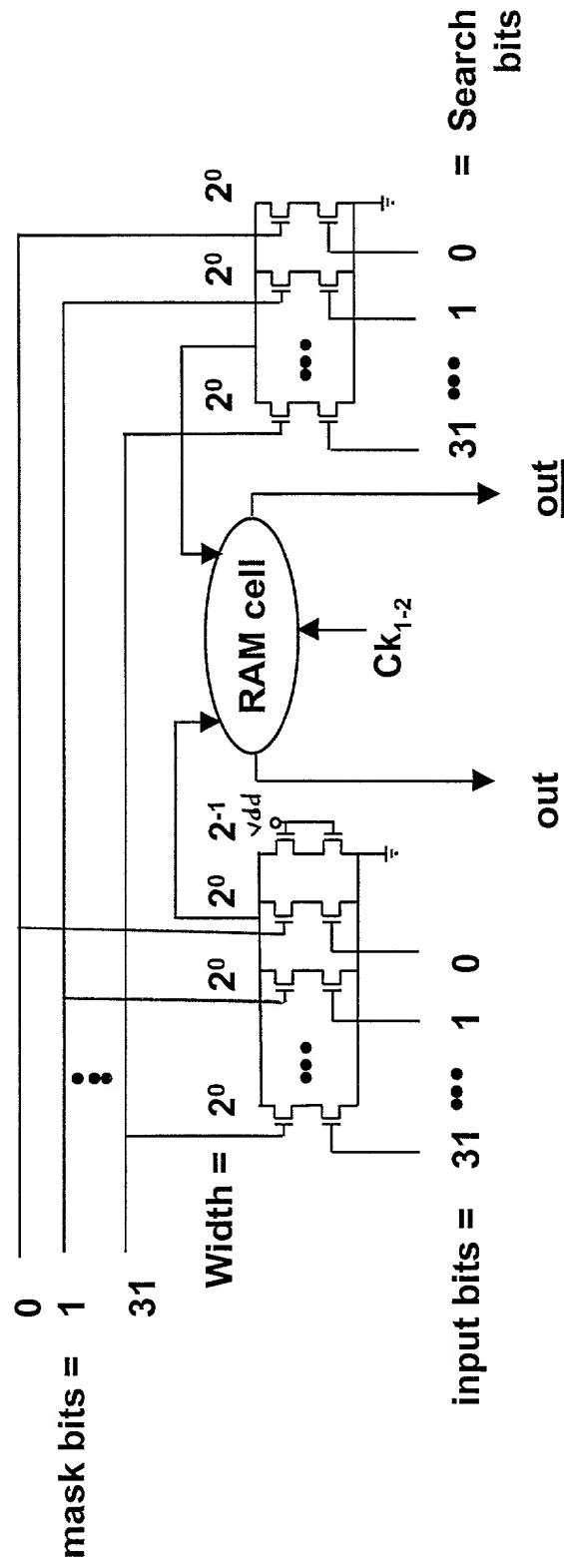


Fig 36

